

What is claimed is:

1. An integrated circuit device having a send/receive macro for serially transferring addresses and data to or
5 from an external device via a serial transfer bus, the integrated circuit device comprising:

a CPU for performing predetermined processing,

wherein

the send/receive macro comprises:

10 a send/receive buffer accessed by the CPU, for storing a plurality of units of data to be transmitted to or received from the serial transfer bus;

an acknowledge detection unit for detecting a data acknowledge signal transmitted from a receiving device in
15 response to transmission of predetermined units of data;
and

a data send unit for transmitting data stored in the send/receive buffer, in response to detection of the data acknowledge signal by the acknowledge signal detection
20 unit, without generating any interrupt to the CPU, and
wherein

the acknowledge detection unit generates a data acknowledge signal non-detection interrupt to the CPU if the acknowledge detection unit does not detect the data
25 acknowledge signal transmitted from the receiving device in response to transmission of the predetermined units of data.

2. The integrated circuit device according to claim 1,
wherein

the data transmission from the data send unit is
5 terminated in response to the data acknowledge signal
non-detection interrupt to the CPU.

3. The integrated circuit device according to claim 1,
wherein

10 when an address acknowledge signal is detected that
is sent by a slave device in response to a transmission
of an address identifying the slave device by the data send
unit as a master, the acknowledge detection unit generates
an interrupt to the CPU.

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4. The integrated circuit device according to claim 1,
wherein

the data send unit initiates serial transmission of
predetermined units of data stored in the send/receive
20 buffer, after an interrupt to the CPU generated when the
acknowledge detection unit detects the address
acknowledge signal.

25 5. The integrated circuit device according to claim 1,
wherein

the serial transfer bus comprises a single data line
and a single clock line, and wherein

the data transfer is carried out serially over the single data line in synchronization with a clock driven onto the clock line.

5 6. An integrated circuit device having a send/receive macro for serially transferring addresses and data to or from an external device via a serial transfer bus,
 the integrated circuit device comprising:
 a CPU for performing predetermined processing,

10 wherein

 the send/receive macro comprises:
 a send/receive buffer accessed by the CPU, for storing a plurality of units of data to be transmitted to or received from the serial transfer bus;

15 a data send unit for transmitting data stored in the send/receive buffer; and

 an arbitration lost detection unit for detecting whether or not, during an address phase in which the data send unit, as a master, serially transmits an address

20 identifying a slave device, an arbitration lost has occurred as a result of concurrent transmission of an address from other master and wherein

 when the arbitration lost detection unit does not detect occurrence of the arbitration lost during the address phase, the CPU stores data to be transferred in the send/receive buffer after the address phase.

7. The integrated circuit device according to claim 6,
wherein

if the arbitration lost detection unit detects
occurrence of the arbitration lost during the address
5 phase, the CPU does not store the data to be transferred
in the send/receive buffer.

8. An integrated circuit device having a send/receive
macro for serially transferring addresses and data to or
10 from an external device via a serial transfer bus,

the integrated circuit device comprising:

a CPU for performing predetermined processing,

wherein

the send/receive macro comprises:

15 a send/receive buffer accessed by the CPU, for storing
a plurality of units of data to be transmitted to or
received from the serial transfer bus;

a data receive unit for receiving data transmitted
via the serial transfer bus and storing the received data
20 in the send/receive buffer; and

an acknowledge signal generation unit for
transmitting a data acknowledge signal to a sending device
in response to reception of the predetermined units of data,
and wherein

25 the acknowledge signal generation unit transmits the
data acknowledge signal on each reception of the
predetermined units of data until reaching to a receivable

data unit count without generating any interrupt to the CPU, and the acknowledge signal generation unit stops transmission of the data acknowledge signal when reaching to the receivable data unit count.

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9. The integrated circuit device according to claim 8, further comprising:

a receive control unit having a receivable count register for storing the receivable data unit count and
10 a counter for counting the receive count each time the data receive unit receives the predetermined units of data, wherein

the acknowledge signal generation unit stops transmitting the data acknowledge signal in response to
15 the count value of the counter reaching the receivable data unit count stored in the receivable count register.

10. The integrated circuit apparatus according to claim 9, wherein

20 the CPU sets the receivable data unit count in the receivable count register.

11. The integrated circuit apparatus according to claim 9, wherein

25 the receive control unit generates an interrupt to the CPU in response to the count value of the counter reaching the receivable data unit count.

12. An integrated circuit device having a send/receive macro for serially transferring addresses and data to or from an external device via a serial transfer bus,

5 the integrated circuit device comprising:

 a CPU for performing predetermined processing,

wherein

 the send/receive macro comprises:

 a send/receive buffer accessed by the CPU, for storing

10 a plurality of units of data to be transmitted to or received from the serial transfer bus;

 a data send/receive unit for receiving data transmitted via the serial transfer bus and storing the received data in the send/receive buffer, and for

15 transmitting the data stored in the send/receive buffer; and

 an access flag register for storing, in the event of an access from the CPU to the send/receive buffer during transmission and reception of the transferring data by the

20 data send/receive unit, a flag indicating occurrence of the access.

13. The integrated circuit device according to claim 12,

wherein

25 the send/receive macro further comprises:

 an acknowledge signal detection unit for detecting a data acknowledge signal transmitted from a receiving

device in response to transmission of the predetermined units of data, and wherein

the data send/receive unit transmits data stored in the send/receive buffer, without generating any interrupt to the CPU, in response to detection of the data acknowledge signal by the acknowledge signal detection unit.

14. The integrated circuit device according to claim 12,
10 wherein

the send/receive macro further comprises
an acknowledge signal generation unit for transmitting a data acknowledge signal to a sending device in response to reception of the predetermined units of data,
15 and wherein

the acknowledge signal generation unit transmits the data acknowledge signal, without generating any interrupt to the CPU, in response to reception of the predetermined units of data, until reaching a receivable data unit count,
20 the acknowledge signal generation unit stops transmission of the data acknowledge signal when reaching to the receivable data unit count.